A study of the threshold voltage in pentacene organic field-effect transistors

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The threshold voltage and carrier mobilities were characterized in pentacene-based organic field-effect transistors with gold top-contact electrodes for different thickness of the pentacene film. The thickness of the semiconductor layer influences the values of the threshold voltage and, to a lesser extent, the saturation current. In this letter, we show that the thickness-dependent part of the threshold voltage results from the presence of an injection barrier at the gold–pentacene contact. We also show how the ratio between the gate insulator thickness and the semiconductor layer thickness alter the value for the saturation current, and therefore produces values for the field-effect mobility that are too low. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1618946]

Organic field-effect transistors (OFETs) have received a lot of attention during recent years.[1–6] Due to the performance levels achieved, they now stand at the point of commercialization,[7–9] just as their organic light-emitting device (OLED) brethren a few years ago. Production techniques have been refined, integrated circuits[10,11] have been realized, even using the now well-renowned technique of ink-jet printing,[12,13] which will have a strong contribution towards lowering production prices for organic circuitry. However, not all the device parameters of OFETs are completely explained, although efforts have been taken to describe them properly; for example, for the parameters that influence the threshold voltage[6,14] or the charge distribution and accumulation in the channel.[15,16] Much research effort has been put forward to meet the challenges involved in describing OFETs properly, and the theory and experimental works have advanced quickly.

An OFET device structure that is commonly used (see Fig. 1) is the so-called bottom-gate, top-contact architecture, sometimes also named staggered geometry. This geometry provides larger contact areas than the bottom-gate, bottom-contact architecture and has been shown to result in better device performance.[17]

In this letter, we present experimental results of pentacene OFETs with gold top contacts with different semiconductor film thicknesses, and we study the thickness effects on the threshold voltage and the channel saturation current. Pentacene/gold is a frequently investigated system in the OFET literature[7,9,18] because of the high hole mobility in pentacene and the high work function of gold. However, an injection barrier of 0.85 eV has recently been found at the gold–pentacene interface, which is higher than expected.[19,20] In another work, it has been observed that the barrier height depends on the deposition sequence, with gold on pentacene yielding up to 1 eV for the injection barrier at the interface.[21] While these references do not completely agree with each other, they do document that a barrier in the range of 0.8 to 1.0 eV exists.

Here, OFETs were built on glass/ITO substrates, where ITO acted as gate electrode. Poly (vinyl alcohol) (PVA), purchased from Aldrich, was spun-cast on top of the ITO as a 120-nm-thick gate dielectric from aqueous solution. Its dielectric constant was measured to be $\epsilon = 5.1$, in good agreement with literature values. Pentacene, also obtained from Aldrich, was thermally evaporated as-is onto the gate dielectric. The deposition speed on the crystal-thickness monitor was 8 Å/s, with a total thickness deposited of 700 nm. Different pentacene thicknesses were obtained by placing the substrates at different positions in the evaporation bloom. The thickness of the pentacene layers was subsequently determined through measurements with a Dektak surface profiler. It was also determined that the roughness of the pentacene film was at the vertical resolution limit of the Dektak surface profiler: 5 nm or less. With the thickness, the deposition rate can be estimated for each device, ranging from less than 0.1 Å/s for the thinnest pentacene layer, to between 4 and 10 Å/s for films between 350 and 930 nm in thickness. It has previously been shown that a deposition rate of 3 to 6 Å/s leads to an optimum mobility with small to negligible variations compared to the experimental error.[22] In a final

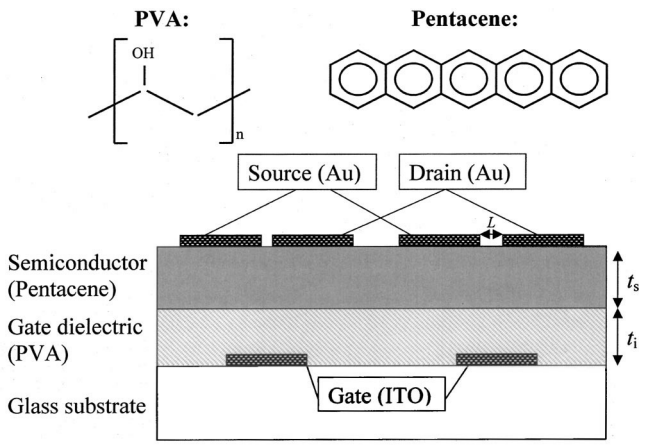

FIG. 1. Top: Chemical structure of the gate dielectric, PVA, and the active semiconductor material, pentacene. Bottom: Device geometry used for the OFET devices.

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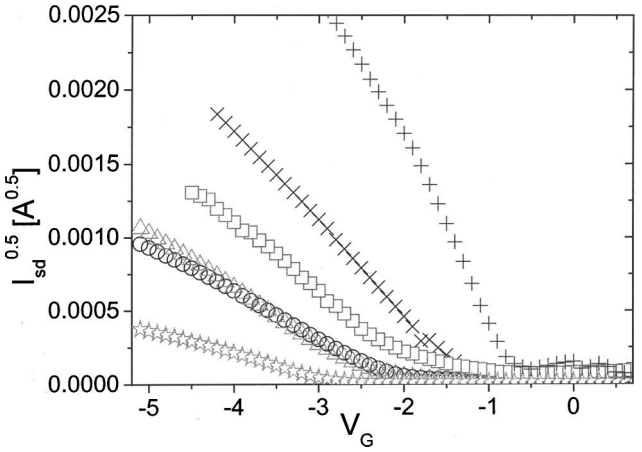

FIG. 2. Transfer characteristic of six OFET devices with different pentacene thicknesses. The gate dielectric was always 120 nm thick. The ordinate shows the square root of the current between the source and drain electrode, the abscissa shows the gate voltage. From bottom left to top right: stars—930 nm pentacene, 60 μm channel length; triangles—700 nm pentacene, 40 μm channel length; circles—500 nm pentacene, 60 μm channel length; squares—400 nm pentacene, 40 μm channel length; cross—355 nm pentacene, 25 μm channel length; plus—30 nm pentacene, 25 μm channel length.

step, gold was thermally evaporated on top of the pentacene layer using shadow masks giving transistors with 25, 40, and 60 μm channel length. The speed of deposition for gold was 0.5 Å/s. The final device can be seen in Fig. 1. Output and transfer characteristics were measured with two source/measure units under vacuum.

Figure 2 shows the transfer characteristic of six different OFET devices, featuring different pentacene film thickness. For the sweeps, the drain voltage was held constant at -7 V to keep the devices in saturation. The curves were measured reproducibly; thus, we did not see any gate dielectric stress effects during the measurements. It is immediately apparent that the threshold voltage at which the transistor is switched on is strongly dependent on the pentacene film thickness. The values of the film thickness, threshold voltage, and mobility are summarized in Table I. The thickness dependence of the threshold voltage shall be the first subject of discussion in this letter.

It is well known that whenever the work function of the metal does not coincide with the valence band (or highest occupied molecular orbital) for p-channel devices, or with the conduction band (or lowest unoccupied molecular orbital) for n-channel devices, an injection barrier with non-ohmic electrical behavior is formed at the metal–semiconductor interface.[16,23,24] This has so far been considered mainly for OLEDs, where a transition between injection-limited electrical behavior at low fields ($E<E_{\text{crit}}$) and transport-limited electrical behavior at high fields ($E>E_{\text{crit}}$) may be observed.[25] However, the source-gate contact in the gold–pentacene system displays an injection barrier, as well, and the injection of charges will also be described by the Fowler–Nordheim (FN) equation[26]

$$j_{\text{FN}} \propto E^2 \exp\left(-\frac{4\sqrt{2qm^*}}{3\hbar}\frac{\phi_B^{1.5}}{E}\right), \tag{1}$$

wherein: j_{FN} is the current density, q is the elementary charge, m^* is the effective mass of a carrier, ϕ_B is the barrier height, and E is the electric field. For a given barrier height and source electrode area, the electrical field at the source–semiconductor interface has to exceed a critical value E_{crit} for the OFET to exhibit saturated field-effect drain current rather than injection–limited current. This will lead to a thickness-dependent injection-barrier contribution $V_{T,\text{inj}}(t)$ to the threshold voltage:

$$V_T(t) = V_T(\Omega) + V_{T,\text{inj}}(t) = V_T(\Omega) + E_{\text{crit}}\epsilon_s t, \tag{2}$$

where $V_T(t)$ is the overall threshold voltage, $V_T(\Omega)$ is the threshold voltage that would remain even for ohmic source–semiconductor contact, $t=t_i+t_s$ is the combined thickness of semiconductor and insulator (here, $t_i=120$ nm=constant), ϵ_s is the semiconductor dielectric constant, and E_{crit} the critical field.

Figure 3 displays the threshold voltages extracted from Fig. 2 plotted against thickness t. We find an approximately linear relationship between V_T and t as predicted by Eq. (2), which confirms that the increased threshold voltage for thicker semiconductor films results from an injection barrier at the gold–pentacene interface. From the fitted line, we find $V_T(\Omega)=-0.4$ V; indeed, most p-type OFETs exhibit slightly negative threshold voltages. From the slope of the fit, we find $E_{\text{crit}}\,\epsilon_s \approx 2.3$ MV/m.

The experimentally obtained curves shown in Fig. 2 were fitted with Eq. (3), and the mobilities of the pentacene transistors were subsequently calculated from the slope:

$$\sqrt{I_{D,\text{sat}}} = \sqrt{\frac{W}{2L}\frac{\mu\epsilon_0\epsilon_i}{t_i}}(V_G - V_T) \tag{3}$$

This equation, where t_i is the thickness of the dielectric, L is the channel length, W is the channel width, and $\epsilon_0\epsilon_i$ is the vacuum permittivity times the insulator dielectric constant, lead to the values in the second to right column in Table I. It can be seen immediately that the mobility is far from constant. While there are different factors contributing to this variation, one of them is most likely due to the fact that the conduction path from the source electrode to the channel is undoped in pentacene, and therefore resistivity can be comparable to that of the insulator. Thus, when we consider the surface charge density Q_A in the accumulation layer:

$$\frac{Q_A}{C_i} = V_i = \epsilon_i E_i t_i, \tag{4}$$

where V_i is the effective voltage at the insulator surface and C_i is the insulator capacitance per area, we find that Q_A

TABLE I. Summary of the values for the threshold voltage and for the mobility for several devices with different pentacene thicknesses. The columns from left to right: t_s is the semiconductor thickness, V_T is the threshold voltage, L is the channel length, and the last two columns contains the mobilities as calculated with Eq. (3) as well as corrected with Eq. (5).

t_s [nm]	V_T [V]	L [μm]	μ_{apparent} [$\text{cm}^2(\text{V s})^{-1}$]	μ_{actual} [$\text{cm}^2(\text{V s})^{-1}$]
30	−0.67	25	0.900	1.13
325	−1.34	25	0.263	0.97
400	−1.66	40	0.239	1.03
500	−2.01	60	0.160	0.82
700	−2.27	40	0.154	1.05
930	−2.69	60	0.041	0.36

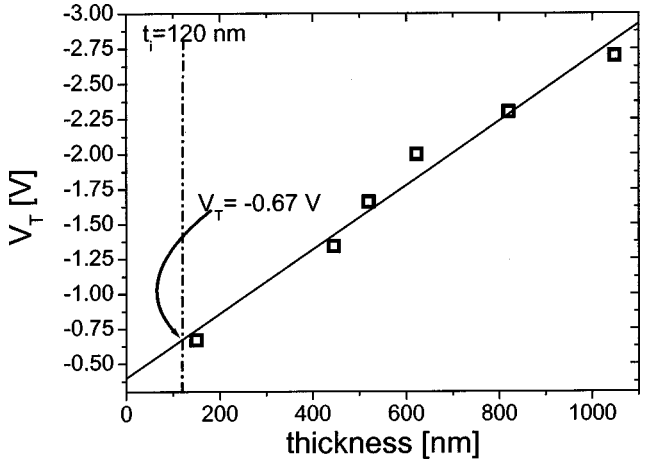

FIG. 3. Linear fit of the threshold voltage versus the thickness of the pentacene layer with Eq. (2). The vertical line indicates the thickness of the gate dielectric of 120 nm, which corresponds to a $V_T(120\ \text{nm}) = -0.67$ V, or a transistor with an infinitely thin layer of pentacene.

depends on the capacitance of the insulator, its thickness, and the field through the insulator. This electric field, however, is described as $E_i = V_G / \epsilon_i [(R_s/R_i) t_s + t_i]$, as the gate voltage drops over both the semiconductor layer (perpendicular to the accumulation layer) and the insulator layer. The factor R_s/R_i weighs the influence of the semiconductor layer according to the relative resistances of the two layers. The fact that the charges have to be transported between the source contact and the channel is the main disadvantage of the staggered device geometry. This is one of the major reasons that dielectrics in OFETs are made to be thicker by usually an order of magnitude than the semiconductor layer. The effect described here, as a matter of fact, is quite known in inorganic FET technologies, in which buried channel devices are known to exhibit less doped accumulation layers.[27] Assuming $R_s \approx R_i$; the saturation current, which is directly proportional to the charges in the accumulation layer, depends on the thickness as follows:

$$I_{D,\text{sat}} \propto Q_A \propto \frac{t_i}{t_s + t_i}. \tag{5}$$

Thus, the saturation current for a given mobility is smaller than expected when using Eq. (3). The mobility values need to be corrected by the inverse of the right-hand side of Eq. (5).

It should be mentioned here that it is highly unlikely that the resistance of the semiconductor is exactly equal to the resistance of the insulator. It is therefore quite conceivable that other factors, such as the slightly different deposition rates, play a role in influencing the mobilities as well. However, just using the factor, we obtain the mobility values in the rightmost column of Table I, which are all within 10% margin, showing very good agreement given normal device fabrication fluctuations. Still, the different deposition rates have influenced the mobilities as well, as shown most prominently with the thickest transistor, exhibiting a mobility lowered by a factor of two. It was controlled to be between 3 and 7 Å/s for all OFETs (as evidenced by a thickness monitor), except for the thickest and the thinnest device. Other channel lengths for the thickest device resulted in comparable mobilities; therefore this explanation seems feasible.

In conclusion, we present a detailed study of the effect of a source–semiconductor injection barrier for the staggered OFET configuration, which was carried out via variation of the semiconductor film thickness. The presence of an injection barrier leads to an increase in the threshold voltage. The increase scales linearly with the thickness of the semiconductor film, which confirms that it corresponds to a transition from injection limited to transport limited behavior. We also show that in the staggered geometry, the saturation currents are influenced for devices with insulating layers thin compared to the semiconductor layer.

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