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Organic field-effect transistors with ultrathin gate insulator

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Abstract

We have used a commercially available Mylar film coated with a thin (≈60 nm) layer of aluminium and an ultrathin (≈3.5 nm) SiO_2 layer as flexible substrate for the manufacture of bottom-gate organic field-effect transistors (OFETs). We show that the SiO_2 layer has insulating properties with a breakdown voltage of 1.6 V and a capacitance of ≈1 μF/cm^2. We have manufactured organic field-effect transistors using this substrate, regioregular poly(3-hexylthiophene) (rrP3HT) as a p-type semiconductor, and gold source and drain contacts. This results in OFETs that operate with voltages on the order 1 V.

Keywords: OFET; Operating voltage; High capacitance; rrP3HT; Aluminium; SiO_2

Transistors using organic semiconductors (organic field-effect transistors, OFETs) have been the focus of intense recent research interest. It is envisaged that the processing advantages of organic semiconductors will lead to applications that are either very cheap, or complement organic display technology. Outstanding examples include inkjet-printed logic circuits [1] and organic active matrix drivers for displays [2].

In many practical situations where cheap 'disposable electronics' products may be applied, cost restrictions will limit the available operational voltage. It is, thus, paramount to develop organic circuits that can operate with low switching voltages. OFET switching voltage is controlled by insulator capacitance and threshold voltage. Capacitance scales inversely with insulator thickness, and threshold voltage often is reduced in thinner insulators. Consequently, the straightforward approach to low voltage OFETs is to minimise gate insulator thickness without the introduction of pinholes. Generally, research into OFET gate insulators has recently received increasing attention [3–8] and is rapidly establishing itself as a line of research equally important for organic electronics as the 'traditional' OFET research themes that address the organic semiconductor itself, and circuit engineering.

We here report on our successful attempts to use a gate insulator of minimum thickness to achieve low operational voltages. We have used a commercially available flexible Mylar film that is coated with a thin (≈60 nm) layer of aluminium which is capped by an ultrathin (≈3.5 nm) SiO_2 layer, as supplied by Flex Products Inc. (Santa Rosa, CA, USA).

The SiO_2 surface was cleaned by spinning-off with HPLC grade methanol and chloroform. For characterisation of the insulating properties of the SiO_2 film, we evaporated 2 mm × 2 mm gold squares. With a commercial capacitance meter working at 800 Hz, we found a capacitance of 0.97 ± 0.05 μF/cm^2 for the Al/SiO_2/Au sandwich, with the variation between measurements on different spots taken as error. Current density/voltage behaviour of the same sandwich were taken with a Keithley 2400 source–measure unit, results are shown in Fig. 1. Dielectric breakdown occurred at 1.6 V in both bias directions.

We subsequently manufactured OFETs by spincasting regioregular poly(3-hexylthiophene) (rrP3HT) from 10 mg/ml solution in chloroform at 1000 rpm onto Mylar/Al/SiO_2 substrates. rrP3HT was purchased from Aldrich and had been dedoped with hydrazine before use. Transistors were completed by shadow mask evaporation of 2 mm wide gold source–drain contacts separated by a 25 μm channel. Through visual inspection, we ensured that the channel region was free of scratches. This lead to a success rate of >75%, i.e. more than three out of four OFETs we manufactured did not display source–drain-to-gate shorts.

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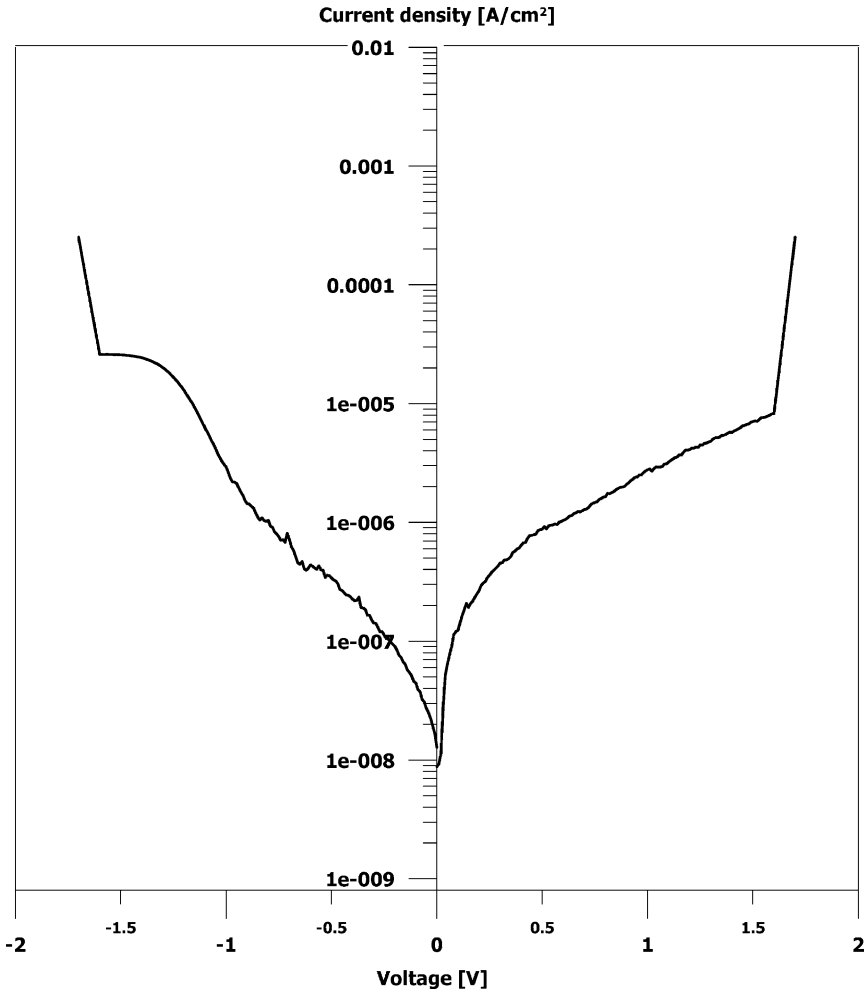

Fig. 1. Current density/voltage characteristic of Al/SiO_2/Au sandwich. Evaporated Au squares had the surface of 0.04 cm^2. Voltage sign refers to aluminium bias with respect to the gold top electrode, which remained earthed.

Transistors were kept under vacuum for >12 h before measurement to reverse the well-known effects of oxygen doping on rrP3HT [9]. Characterisation was carried out under nitrogen atmosphere using two Keithley 2400 source–measure units controlling source–drain and gate voltage, respectively. Fig. 2a shows the output characteristic for gate voltages up to −1.5 V, which is close to, but below, the insulator breakdown. Fig. 2a also shows the gate leakage current density. Gate leakage reduces as V_D is ramped; $j_G(V_D = V_G) \approx 1/2 j_G$ ($V_D = 0$). This is because at $V_D = 0$, we have leakage from both source and drain to gate, but at $V_D = V_G$, only from source to gate. Fig. 2b shows transfer characteristics of the same transistor in the linear ($V_{SD} = -0.1$ V) and saturation ($V_{SD} = -1$ V) regime. Characteristics are clearly recognisable as typical for p-type OFETs. Remarkably, transistors operate with very low voltages in the order of 1 V. This is considerably lower than previously reported 'low voltage' OFETs [10], and within the range of commercial 1.5 V batteries.

Carrier mobilities in the saturation regime were determined in two ways: firstly, from sweeps where gate- and drain-voltage were ramped simultaneously ($V_G = V_D$); and secondly, from the saturated transfer characteristic. Fig. 3 shows the two results in the appropriate plot, $\sqrt{I_D}$ versus V_G, which according to theory, should give a straight line above threshold with a slope proportional to mobility. However, close to threshold, both lines in Fig. 3 display curvature rather than a linear rise. This may be the result of a gate voltage dependent mobility. It is established that carrier mobilities depend on the charge density Q_S in the accumulation layer, with mobility increasing with increasing Q_S as the semiconductor DOS is gradually filled, and levelling off to a constant mobility at high Q_S [10]. We have, therefore, fitted straight lines to the high gate voltage region of the plots. The high gate voltage slope in Fig. 3 corresponds to a mobility $\mu = 1.3 \times 10^{-3}$ $cm^2/(V\,s)$, with very little difference between the two data sets. Mobilities were reproducible within the range $(1.1–1.4) \times 10^{-3}$ $cm^2/(V\,s)$ for different transistors. The rrP3HT mobility found here is at the lower end of the range of mobilities reported for rrP3HT on SiO_2 previously [11]. The mobility may be improved by the now customary chemical treatment of SiO_2

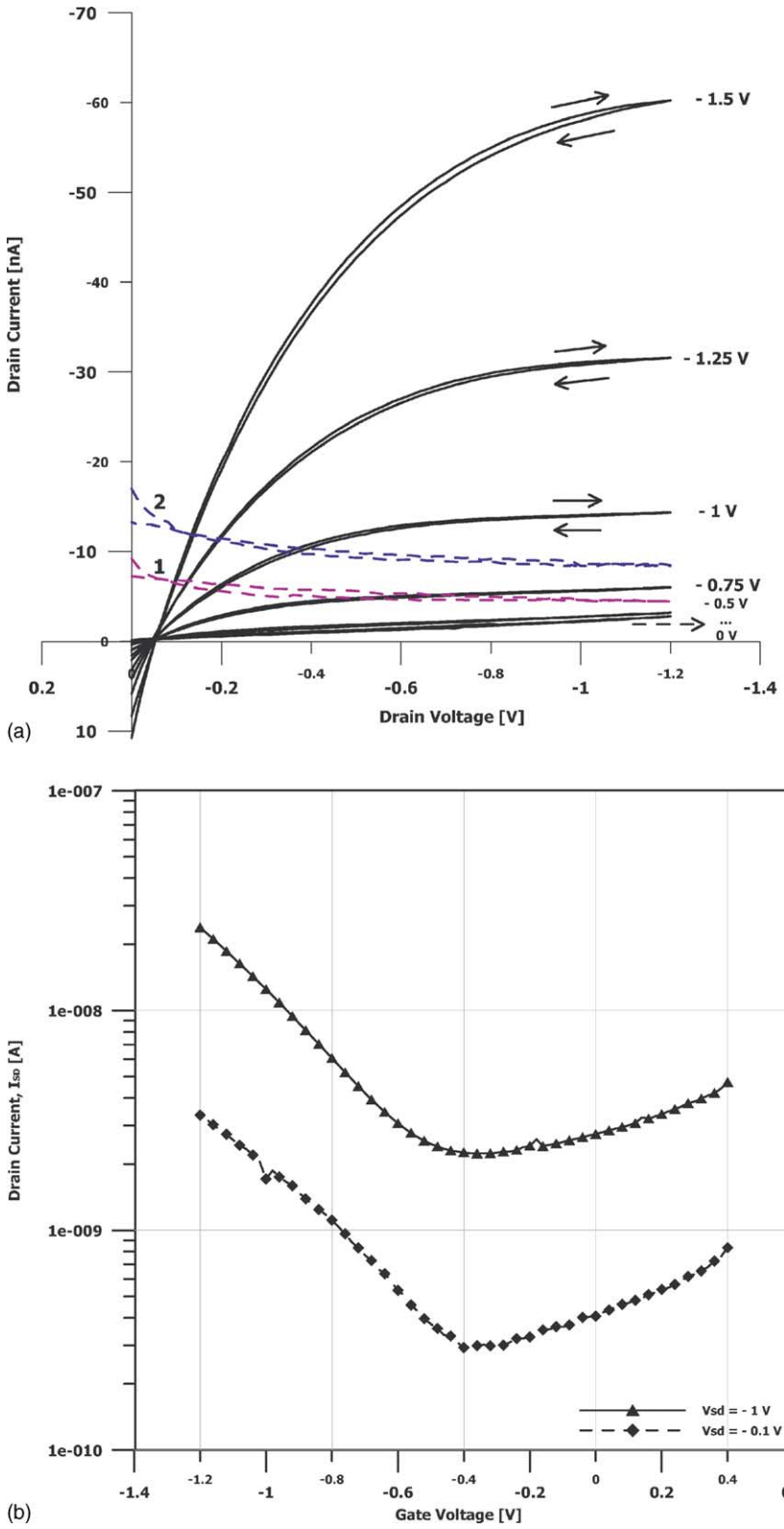

Fig. 2. (a) Output characteristics of OFETs using regioregular poly(3-hexylthiophene) on commercial Mylar/Al/SiO_2 substrate, 2 mm × 2 mm source and drain gold top contacts were used. Dashed lines are gate leakage current at two selected gate voltages (1, $V_G = -1$ V; 2, $V_G = -1.25$ V). (b) Saturated and linear transfer characteristics of same device on logarithmic scale.

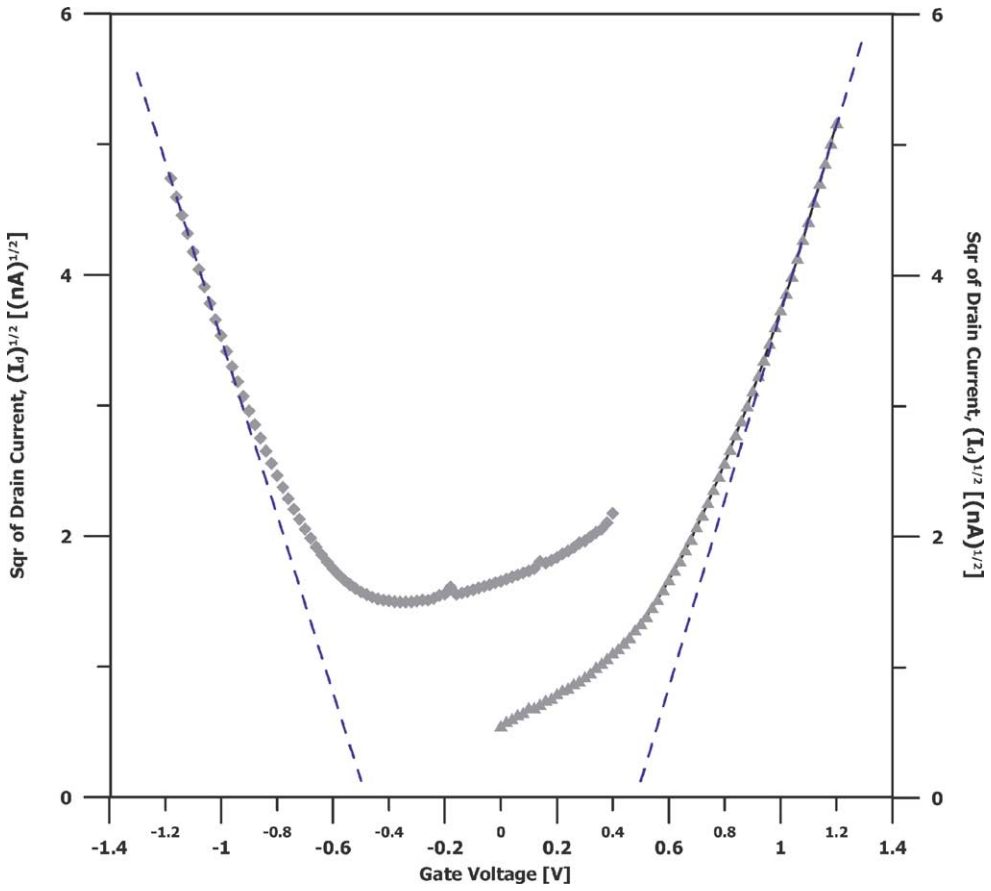

Fig. 3. Square root of drain current vs. gate voltage plot for the data from the saturated transfer characteristic (Fig. 2b, diamonds), and for scans wherein drain- and gate-voltage were ramped simultaneously ($V_D = V_G$) (triangles).

surfaces [12]. Threshold voltage was extracted from the $V_G = V_D$ sweep, because in this mode, drain–gate leakage is zero and the measured drain current is not affected by leakage. We find $V_T = -0.44$ V, giving normally-off OFETs.

In summary, we have shown that commercially available Mylar/Al/SiO_2 film can serve as flexible substrate for OFETs that requires no post-purchase preparation steps. If visible scratches in the metalised surface are avoided, we rarely encounter pinholes and OFET manufacture is rather reliable and reproducible. Due to low gate insulator thickness, we arrive at high capacitance, low operational voltage OFETs. Mobility is moderate and increases with gate voltage. Further work will address the modification of the insulator surface with a self-assembling monolayer (SAM), which often improves mobility.

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